

1 What is claimed is:

Sub A3
1 1. A direct current sum bandgap voltage comparator
2 comprising:

3 a summing node;

4 a plurality of current sources connected to the
5 summing node, each current source supplying a current to
6 the summing node and being connected to a power supply
7 voltage, wherein the current at the summing node is equal
8 to zero when the power supply voltage is equal to a
9 preselected voltage; and

10 an indicator circuit having an input connected to the
11 summing node and generating a logical signal at an output,
12 responsive to voltage changes in the summing node.

1 2. The direct current sum bandgap voltage comparator of
2 claim 1, wherein the current sources supply currents
3 according to a band-gap equation.

1 3. The direct current sum bandgap voltage comparator of
2 claim 2, wherein the band-gap equation is:

3
$$K_1 (V_{CC} - V_T) + K_1 V_T = K_2 V_{BE} + K_3 (kT/q)$$

1 where V_{CC} is the power supply voltage, V_T is the threshold
2 voltage, V_{BE} is the base emitter voltage, and kT/q is equal
3 to the threshold voltage, V_T , where k is Boltzman's
4 constant, T is the temperature in kelvin, q is the
5 electronic charge, and K_1 , K_2 , and K_3 are constants.

1 4. The direct current sum bandgap voltage comparator of
2 claim 3, wherein the plurality of current mirrors comprises
3 four current mirrors.

1 5. The direct current sum bandgap voltage comparator of
2 claim 4, wherein the first current mirror includes a
3 plurality of transistors and supplies a current to the
4 summing node defined by $K_1(V_{CC} - V_T)$, where V_{CC} is the power
5 supply voltage and V_T is a threshold voltage in the first
6 current mirror.

1 6. The direct current sum bandgap voltage comparator of
2 claim 5, wherein the second current mirror includes a
3 plurality of transistors and supplies a current to the
4 summing node defined by $K_1 V_T$, where V_T is a threshold voltage
5 in the second current mirror.

1 7. The direct current sum bandgap voltage comparator of
2 claim 6, wherein the third current mirror includes a
3 plurality of transistors and supplies a current to the
4 summing node defined by $K_2 V_{BE}$, where V_{BE} is a base-emitter
5 voltage defined by a selected transistor in the third
6 current mirror.

1 ~~7~~ 8. The direct current sum bandgap voltage comparator of
2 claim ~~6~~ 7, wherein the fourth current mirror supplies a
3 current to the summing node defined by $K_3 (kT/q)$.

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1 9. The direct current sum bandgap voltage comparator of
2 claim 8 further comprising a clamping circuit connected to
3 the summing node, wherein a voltage swing, responsive to
4 changes in current supplied by the current mirrors, may be
5 selected for the summing node.

1 10. The direct current sum bandgap voltage comparator of
2 claim 8 further comprising a cascode stage interposed
3 between the summing node and the current mirrors.

1 ~~10~~ 11. The direct current sum bandgap voltage comparator of
2 claim ~~8~~ 7 further comprising a hysteresis circuit, connected
3 to the indicator circuit to reduce noise.

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1 ¹¹¹~~12~~. The direct current sum bandgap voltage comparator of
2 claim ⁷¹~~8~~, wherein the indicator circuit includes a pair of
3 inverters connected in series, wherein an input in the
4 first inverter is the input of the indicator circuit
5 connected to the summing node and an output of the second
6 inverter is the output of the indicator circuit.

1 ¹¹²~~13~~. The direct current sum bandgap voltage comparator of
2 claim ¹¹²~~12~~, wherein the indicator circuit provides a logic
3 one output if the power supply is equal to or greater than
4 a preselected voltage.

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1 22. The zero power circuit of claim 21, wherein the fourth
2 current mirror supplies a current to the summing node
3 defined by $K_3(kT/q)$.

1 23. The zero power circuit of claim 22 further comprising
2 a clamping circuit connected to the summing node, wherein
3 a voltage swing, responsive to changes in current supplied
4 by the current mirrors, may be selected for the summing
5 node.

1 24. The zero power circuit of claim 22 further comprising
2 a cascode stage interposed between the summing node and the
3 current mirrors.

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1 25. The zero power circuit of claim 22 further comprising
2 a hysteresis circuit connected to the indicator circuit to
3 reduce noise.

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1 26. The direct current sum bandgap voltage comparator of
2 claim 22, wherein the indicator circuit provides a logic
3 one output if the power supply is equal to or greater than
4 a preselected voltage.

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A 6
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I 7

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A 5
1 14. A zero power circuit comprising:

2 a first circuit;

3 a direct current sum bandgap voltage comparator
4 comprising:

5 a summing node;

6 a plurality of current sources connected to the
7 summing node, each current source supplying a current to
8 the summing node and being connected to a power supply
9 voltage, wherein the current at the summing node is equal
10 to zero when the power supply voltage is equal to a
11 preselected voltage; and

12 an indicator ~~circuit~~ having an input connected to
13 the summing node and generating a logical signal at an
14 output, responsive to changes in the summing node; and

1 a switching circuit for providing power to the first
2 circuit from a primary power supply and a secondary power
3 supply, the switching circuit being connected to the output
4 of the indicator circuit, wherein power from the primary
5 power supply is supplied to the first circuit if the
6 logical signal indicates that the power supply voltage is
7 equal to or greater than the preselected voltage and power
8 from the secondary power supply is supplied to the first
9 circuit if the power supply voltage is less than the
10 preselected voltage.

1 15. The zero power circuit of claim 14, wherein the
2 current sources supply currents according to a band-gap
3 equation.

1 16. The zero power supply circuit of claim 15, wherein the
2 band-gap equation is:

3
$$K_1 (V_{CC} - V_T) + K_1 V_T = K_2 V_{BE} + K_3 (kT/q)$$

1 where V_{CC} is the power supply voltage, V_T is the threshold
2 voltage, V_{BE} is the base emitter voltage, and kT/q is equal
-3 to the thermal voltage, where k is Boltzman's constant, T
-4 is the temperature in kelvin, q is the electronic charge,
-5 and K_1 , K_2 , and K_3 , are constants.

1 17. The zero power circuit of claim 16, wherein the
2 plurality of current mirrors comprises four current
3 mirrors.

1 18. The zero power circuit of claim 16, wherein the
2 secondary power supply is a battery.

1 19. The zero power circuit of claim 17, wherein the first
2 current mirror includes a plurality of transistors and
3 supplies a current to the summing node defined by $K_1(V_{CC} - V_T)$,
4 where V_{CC} is the power supply voltage and V_T is a threshold
5 voltage in the first current mirror.

1 20. The zero power circuit of claim 17, wherein the second
2 current mirror includes a plurality of transistors and
3 supplies a current to the summing node defined by $K_1 V_T$,
4 where V_T is a threshold voltage in the second current
5 mirror.

1 21. The zero power circuit of claim 20, wherein the third
2 current mirror includes a plurality of transistors and
3 supplies a current to the summing node defined by $K_2 V_{BE}$,
4 where V_{BE} is a base-emitter voltage defined by a selected
5 transistor in the third current mirror.